CLAIMS

I claim:

1. A method comprising synchronizing interrupts of a processor with signals from a wireless link synchronization unit.

2. The method as in claim 1, comprising synchronizing interrupts of said processor with signals from a slot timer.

3. The method as in claim 1, comprising scheduling interrupts of said processor in advance of slot signals issued by said wireless link synchronization unit

4. The method as in claim 1, comprising dividing a function into at least two or more segments wherein a segment may be processed to completion by said processor within the time available in a slot.

5. The method as in claim 4, comprising dividing a background function into two or more segments.

6. A method comprising prohibiting interrupts of a processor during a slot other than interrupts by a command scheduled for processing during said slot.

7. The method as in claim 6, comprising scheduling, prior to the start of said slot, said command to be processed by said processor during said slot.

8. The method as in claim 7, wherein said scheduling comprises selecting a background command to be processed by said processor during said slot.

9. The method as in claim 8, wherein scheduling said background command comprises selecting a load estimation command.

10. The method as in claim 8, wherein said selecting said background command comprises selecting a segment of said background command to be processed during said slot.

11. The method as in claim 6, comprising selecting said command to be processed by said processor on the basis of a pre-determined priority among commands waiting to be processed by said processor.

12. The method as in claim 6, comprising masking a signal of a slot timer during a processing of a transmit command.

13. The method as in claim 6, comprising storing in a data storage unit an indication of commands waiting to be processed by said processor.

14. The method as in claim 13, comprising storing in a second data storage unit an indication of a slot timer signal that may interrupt said processor during said slot.

15. The method as in claim 14, comprising comparing a value stored in a designated position of said data storage unit with a value stored in a designated position of said second data storage unit.

16. A method comprising dividing a background function into segments, wherein each segment is capable of being processed by a processor to completion within a time period of a slot.

17. The method as in claim 16, comprising:

processing a segment of said background command during a slot; and

permitting an interrupt of a processor by a command other than said background command during a subsequent slot and prior to the completion of processing of a predetermined number of said segments of said background command.

18. The method as in claim 17, wherein said permitting an interrupt of said command other than said background command comprises evaluating a priority of said command compared to a priority of said background command.

19. A method comprising delaying during a slot an interruption of a processor.

20. The method as in claim 19, comprising scheduling, prior to the start of said slot, a command to be processed by said processor during said slot

21. The method as in claim 19, wherein said delaying comprises delaying an interrupt of said processor during the processing of a background command.

22. The method as in claim 19, comprising dividing a background command into segments, said segments capable of being processed to completion within the time available in a slot.

23. An article comprising a data storage unit having stored thereon instructions that when executed by a processor, result in synchronizing interrupts of a processor with timing signals from a wireless link synchronization unit.

24. The article as in claim 23, wherein said instructions further result in synchronizing said interrupts to the timing signals of a slot timer.

25. The article as in claim 23, wherein said instructions further result in scheduling interrupts of said processor in advance of slot signals issued by said wireless link synchronization unit.

26. A communication device comprising:

a dipole antenna; and a

a state machine to synchronize interrupts of a processor with timing signals from a wireless link synchronization unit.

27. The communication device as in claim 26, wherein said wireless link synchronization unit comprises a slot timer.

28. The communication device as in claim 26, comprising a register to store an indication of a background function waiting to be processed.

29. An apparatus comprising:

a host; and

a controller,

said controller to prohibit interrupts of a processor during a slot other than by a command scheduled for processing during said slot.

30. The apparatus as in claim 29, wherein said controller is to schedule, prior to the start of said slot, said command to be processed by said processor during said slot.

31. The apparatus as in claim 29, wherein said controller is to select a background command to be processed by said processor during said slot.

32. A system comprising

a network interface card; and

a controller;

said controller to divide a background command into segments, each of said segments capable of being processed to completion by a processor within the time period of a slot.

33. The system as in claim 32, comprising:

a processor to process to completion a segment of said background command during said slot; and

said controller capable of permitting an interrupt of said processor by a command other than said background command during a subsequent slot and prior to the completion of processing of all of said segments of said background command.

34. The system as in claim 33, said controller to evaluate a priority of said command other than said background command compared to a priority of said background command.

35. A device comprising a controller to delay an interrupt of a processor during a slot.

36. The device as in claim 35, said controller to schedule, prior to the start of said slot, a command to be processed by said processor during said slot.

37. The device as in claim 35, said controller to divide a background command into segments, said segments capable of being processed to completion by said processor within the time available in said slot.